Product Brochure

Anritsu envision : ensure

High-Speed Serial Data Test Solution

High-Speed Serial Data Test Software	MX183000A
Signal Quality Analyzer-R	MP1900A*
Signal Quality Analyzer	MP1800A

*: Refer to the MP1900A PCIe/USB/Thunderbolt Test Solution Catalog (MP1900A-J-A-1) for the latest information on MP1900A high-speed-bus test solutions.

Test Target: All Serial IF

High-Speed Serial Data Test Solution

100G Ethernet　PCI express　USB　Thunderbolt

SQA/SQA-R — For Evaluating Both Internal and External Digital Equipment Interfaces

Digital equipment interfaces are becoming faster as well as adopting serial data transmissions to handle the large data volumes required by the spread of cloud computing applications and transmission of high-resolution graphics such as 4k/8k. Large-capacity interfaces such as PCI Express, USB, Thunderbolt, etc., used by digital equipment are being upgraded to faster PCI Express 4.0 (16 GT/s) and starting discussion of Gen5, USB3.1 Gen2 (10 Gbit/s), Thunderbolt (20 Gbit/s), etc.
In addition, these interfaces are also becoming multi-channel and support for multiple interfaces in a single unit is also required, which necessitates assured signal integrity for each interface.
The MP1800A/MP1900A are a total measurement solution for assuring standards compliance of high-speed digital interfaces such as PCI Express, USB, Thunderbolt, etc., at every stage from development through to mass production, and cutting the time for verifying Jitter test margins.

MP1800A SQA
MP1900A SQA-R

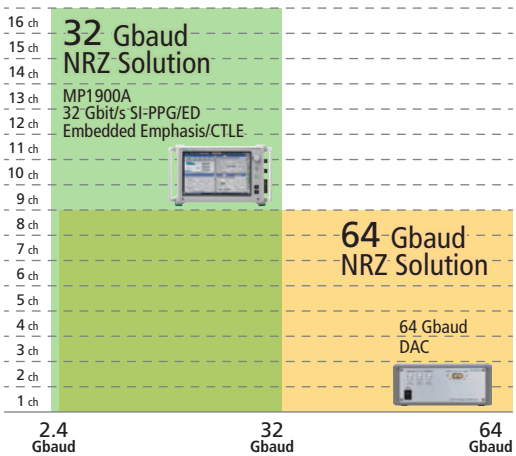
Supports automatic and multi-channel BER and Jitter measurements of equipment external and internal interfaces interfaces

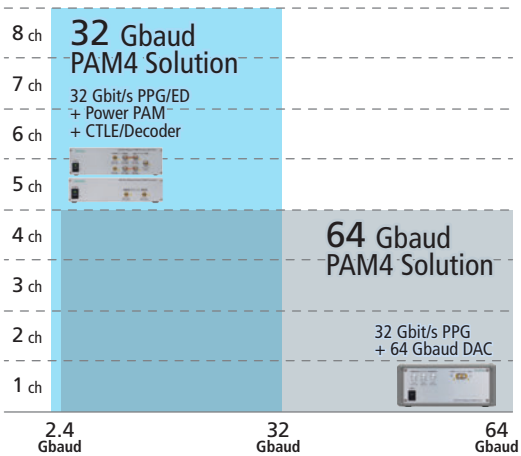
The Signal Quality Analyzer-R MP1900A and the Signal Quality Analyzer MP1800A are a modular type bit error rate tester (BERT). It has a built-in pulse pattern generator (PPG) for outputting high-quality, wideband multi-channel NRZ signals at 2.4 Gbit/s to 32.1 Gbit/s, an error detector (ED) with high input sensitivity, and a Jitter modulation source supporting Jitter Tolerance tests; it supports PAM4 modulation and is ideal for evaluating transmissions of external interfaces such as next-generation Ethernet.

Multi-channel NRZ solutions

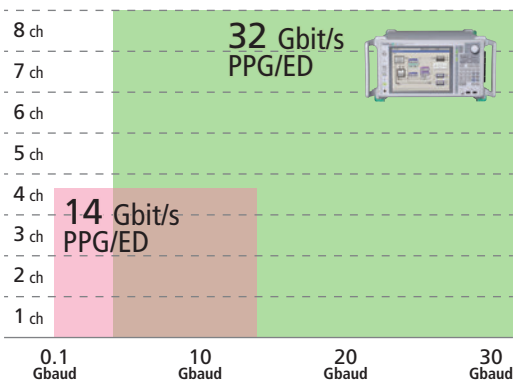
Multi-channel PAM4 solutions

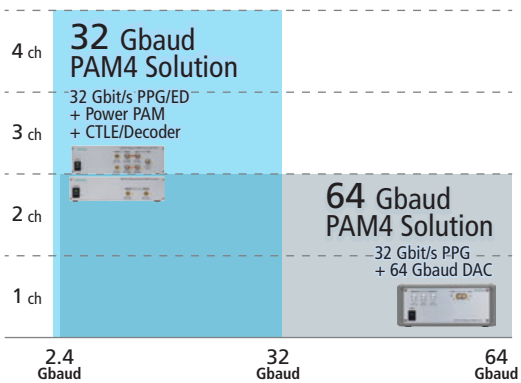
MP1900A



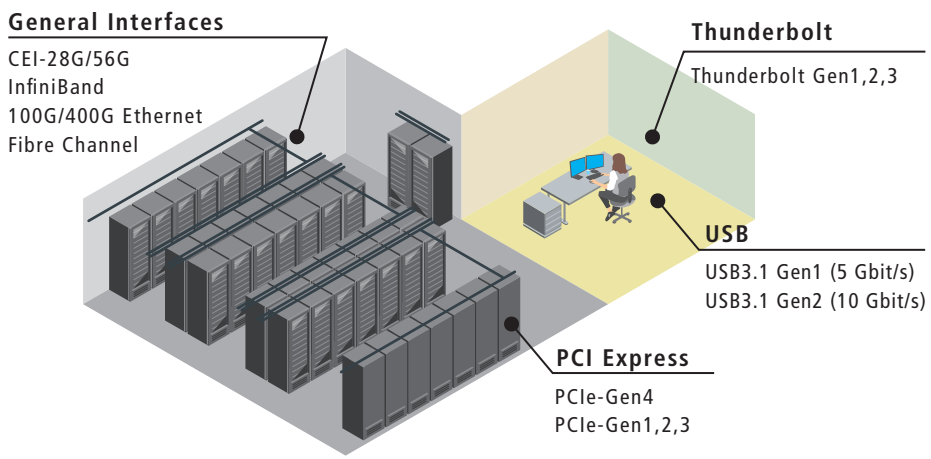


MP1800A





Target Applications



Various Applications

Supports internal and external interfaces, such as Ethernet, PCI Express, as well as USB3.1/ Thunderbolt via USB Type-C connector and cables.

Supports Calibration of Stressed Signals, Device Status Transition using Link Sequence, Jitter Tolerance Tests

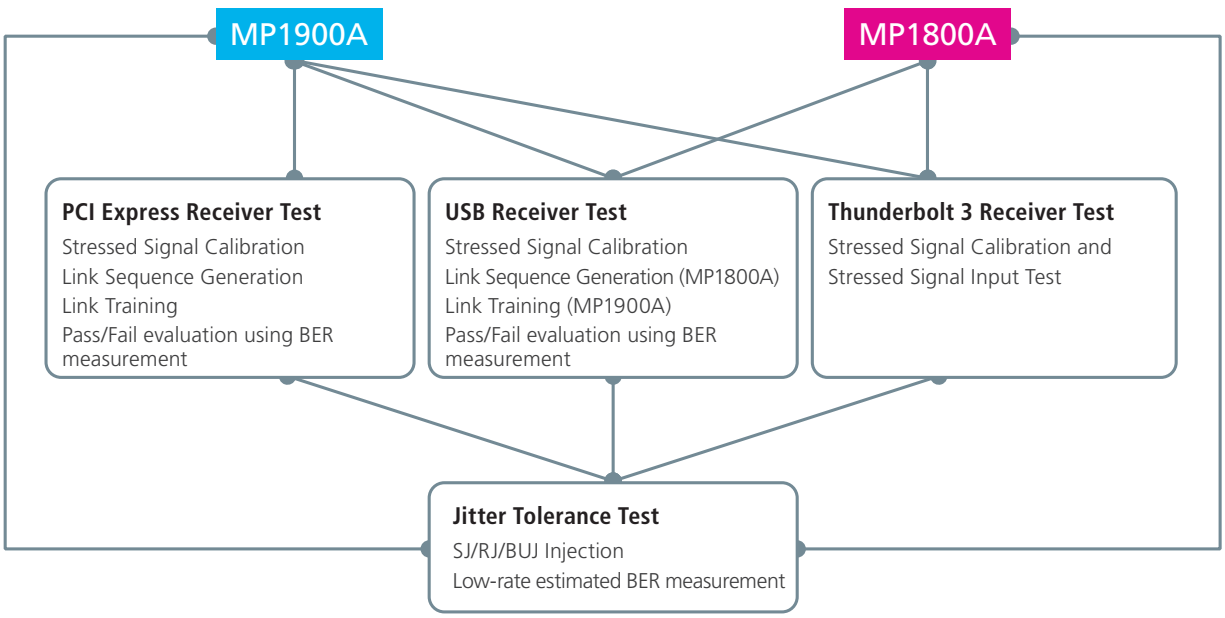
When used in combination with the High-Speed Serial-data Test Software MX183000A and GRL Corporation's automation software, it supports high-efficiency design verification of high-speed PCI Express, USB, and Thunderbolt receivers.
Anritsu's MP1900A and MP1800A are a one-stop solution for evaluating high-speed, multi-channel, NRZ/PAM4 digital equipment internal and external interfaces. It is ideal for configuring automatic measurement systems with high reproducibility to shorten design verification times.

MX183000A Software

Calibration of stressed signal	Transition DUT state to Loopback	Stressed Receiver Testing
Stressed Signal Calibration	PCIe/USB Link Sequence Generation Function PCIe/USB Link Training Function	Jitter Tolerance Test
Supports all-in-one automatic measurement from calibration of stressed input signal to testing to shorten design verification period. *: Supported by GRL Corporation Automation Software	Generates Link Sequence required by PCI Express and USB receiver tests for transitioning device to Loopback status.	Supports signal integrity tests such as Jitter Tolerance tests. Supports injection of various Jitter types and CM/DM into low-Intrinsic-Jitter and low-distortion Data signals, as well as Emphasis and ISI control and generation of various test signals

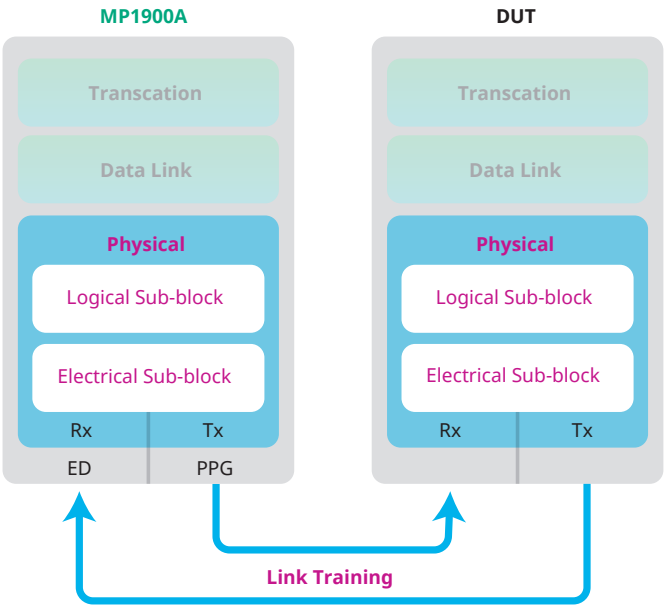
MP1900A/MP1800A Hardware

Multi-channel BER Measurements | High-quality PPG/ High-input-sensitivity ED | PAM4 BER Measurements | Emphasis | Jitter/Noise Generation



Installing MX183000A software in the MP1800A/MP1900A supports generation of Link Sequence patterns required for evaluation of PCI Express and USB devices and Jitter Tolerance tests.

The MX183000A can be used for SERDES IC Jitter Tolerance tests as well as for tests of digital equipment internal and external interfaces by the Link Sequence Generation and Link Training Function, required for evaluation of devices supporting next-generation PCI Express and USB standards.

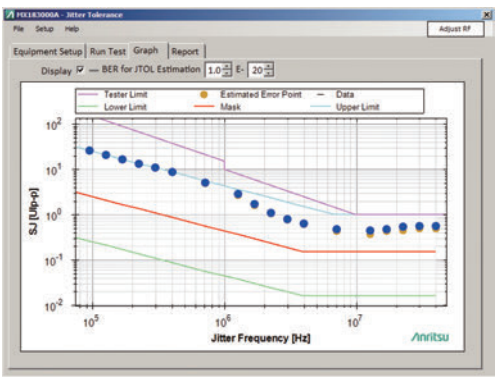


Supports physical layer measurements of add-in cards and system boards

- Tx/Rx Link Equalization Response Test
- Rx Link Equalization Test
- Receiver Jitter Tolerance Test

Jitter Tolerance Test Function (MX183000A-PL001) MP1800A MP1900A

- Supports versatile Jitter Tolerance measurements
- Injects SJ/RJ/BUJ for PHY device Jitter Tolerance tests
- Supports Mask measurements for various standards
- Shortens measurement time using low-error-rate (1E-12, 1E-15, etc.) estimation function
- Uses Binary, Upward, Downward, and Binary + Linear capture methods to measure tolerance points dependent on device characteristics



Low-Rate Estimated BER Measurement

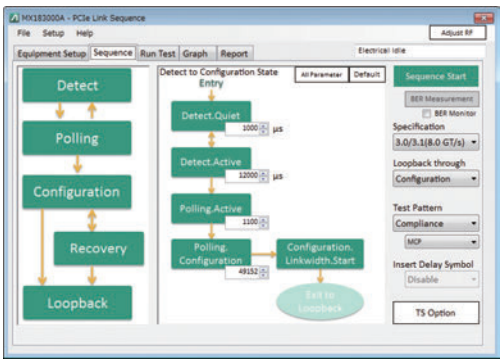
PCI Express

Measurement Item	Supported Software
Transmitter Test	*
Stressed Signal Calibration	*
Transition to Loopback State	MX183000A (Option PL011, PL021)
Tx Response Time	MX183000A (Option PL021)
Rx Link Equalization Test	MX183000A (Option PL021)
Jitter Tolerance Test	MX183000A (Option PL001, Jitter Tolerance Margin Measurement)
PLL loop Bandwidth Test	*

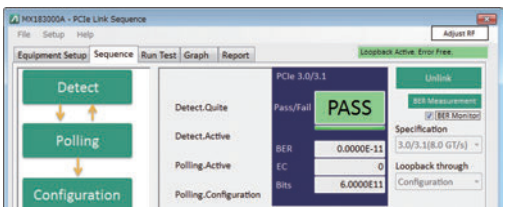
*: Please Contact our Sales Section about MP1900A support.

PCI Express Link Sequence Generation Function (MX183000A-PL011) MP1800A MP1900A

- Uses training sequence generation to set PCI Express Gen 1 to 4 devices to Loopback state
- Automates Pass/Fail evaluation of devices transitioned to Loopback state
- Generates 8B/10B, 128B/130B, Scramble, SKIP Insertion



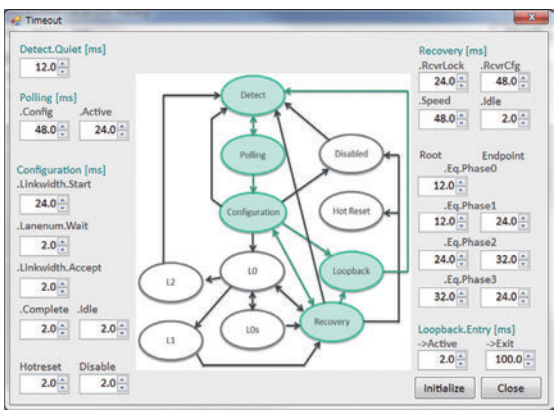
LTSSM Parameter Setting Screen



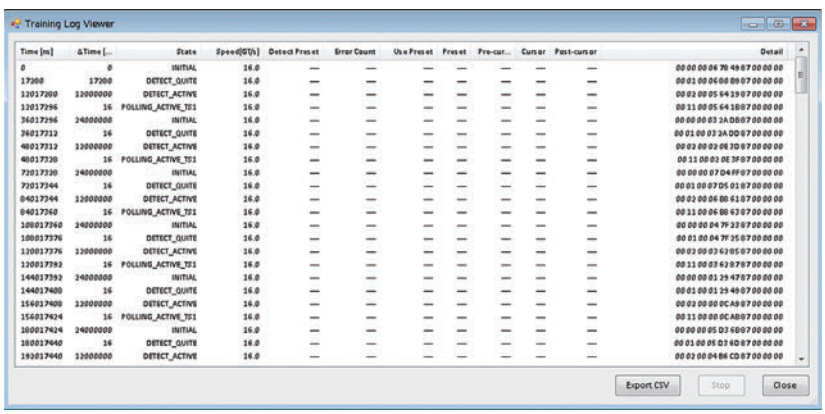
Pass/Fail Screen

PCI Express Link Training (MX183000A-PL021) MP1900A

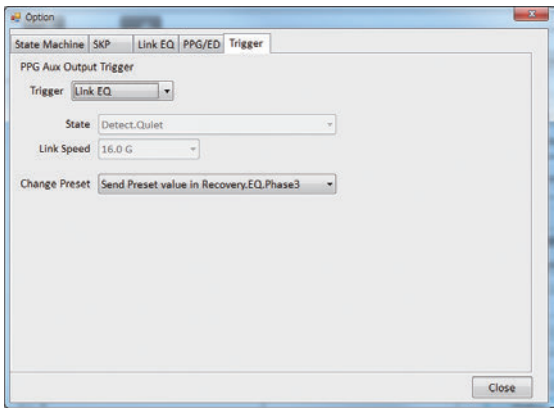
- Support for Protocol Awareness PCIe Gen1 to Gen5 receiver tests
- Link Training and LTSSM analysis functions
- Generates LTSSM transition event trigger for Tx response time test and troubleshooting



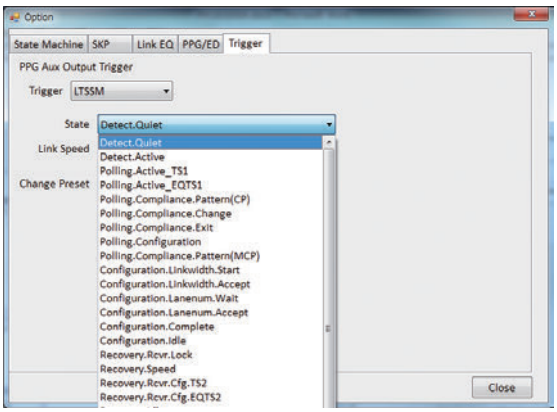
Link Training State transitions



LTSSM log of each LTSSM state transition



Generates Tx response time test trigger



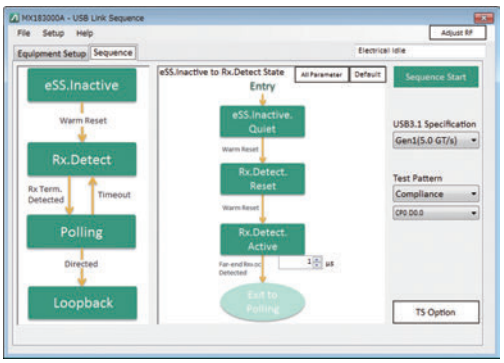
Generates LTSSM state transition event trigger

USB

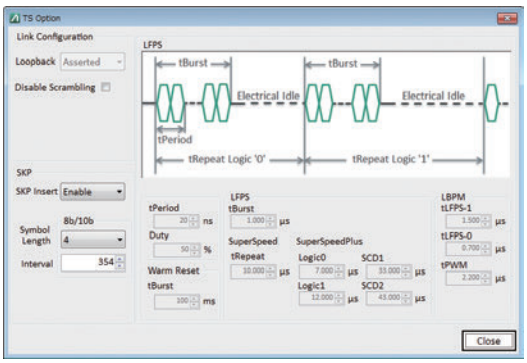
Measurement Item	Supported Software
Stressed Signal Calibration	GRL-USB31-RXA
Transition to Loopback State	MX183000A (Option PL022), MX183000A (Option PL012)
Jitter Tolerance Test	MX183000A (Option PL001), GRL-USB31-RXA

USB Link Sequence Generation Function (MX183000A-PL012) MP1800A

- Sets Link Sequence, type, and test pattern, and transitions to Loopback mode for evaluating USB3.1 Gen1, Gen 2 devices
- Generates 8B/10B, 128B/132B, Scramble, SKIP Insertion, LFPS



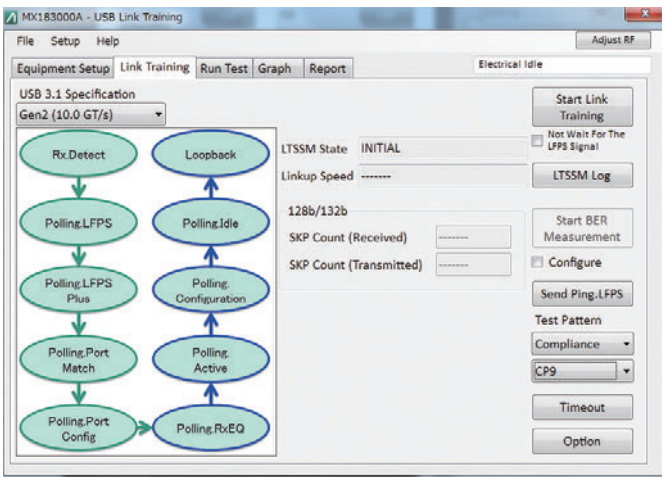
Link Sequence Setting Screen



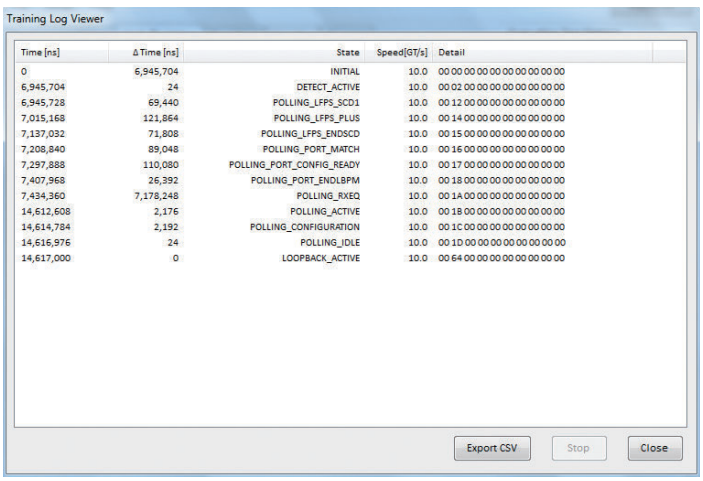
LFPS Setting Screen

USB Link Training (MX183000A-PL022) MP1900A

- Support for Protocol Awareness USB3.1 Rx Test Solution
- Link Training and LTSSM analysis functions



Controls transition to Loopback (Link Training function)



LTSSM log of each LTSSM state transition

GRL Automated Test Solution Series

The Granite River Labs (GRL) software packages for the Signal Quality Analyzer MP1800A automate receiver tests for high-speed serial- bus interfaces. These software packages control the MP1800A noise generation signal source, variable ISI channel, and real-time oscilloscope to automate the complex calibration for high-speed serial-bus receiver tests and Jitter Tolerance test, cutting the testing burden for engineers.

GRL Application Software

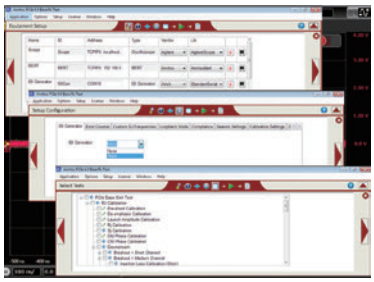
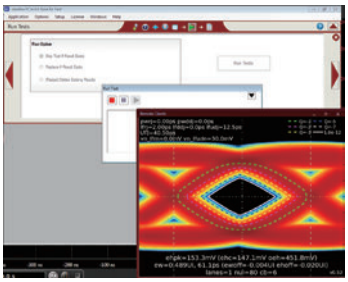
Supported Standard	Name
PCI Express 4.0	GRL-PCIE4-BASE-RXA
USB 3.1	GRL-USB31-RXA
Thunderbolt 3	GRL-TBT3-RXA

Features

- Controls each measuring instrument to simplify Eye Opening calibration, measurement conditions settings, and test execution
- Calibrates test signal with high reproducibility and executes receiver test
- Automates standards-compliant Jitter and amplitude Pass/Fail evaluations

GRL-PCIE4-BASE-RXA

Automates measurement of PCIe-Gen4 Rev 0.5 devices.

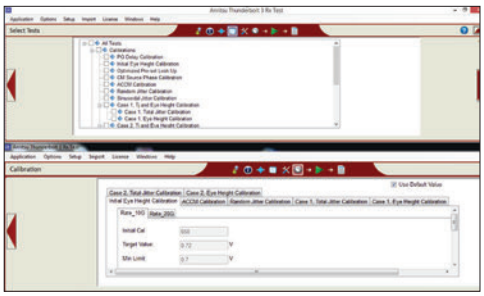
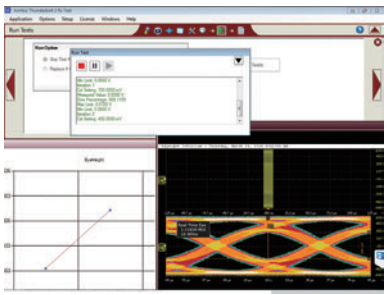
Calibration Setting and Measurement Screens

GRL-USB31-RXA

Automates USB3.1 Gen1/Gen2 device measurements

GRL-TBT3-RXA

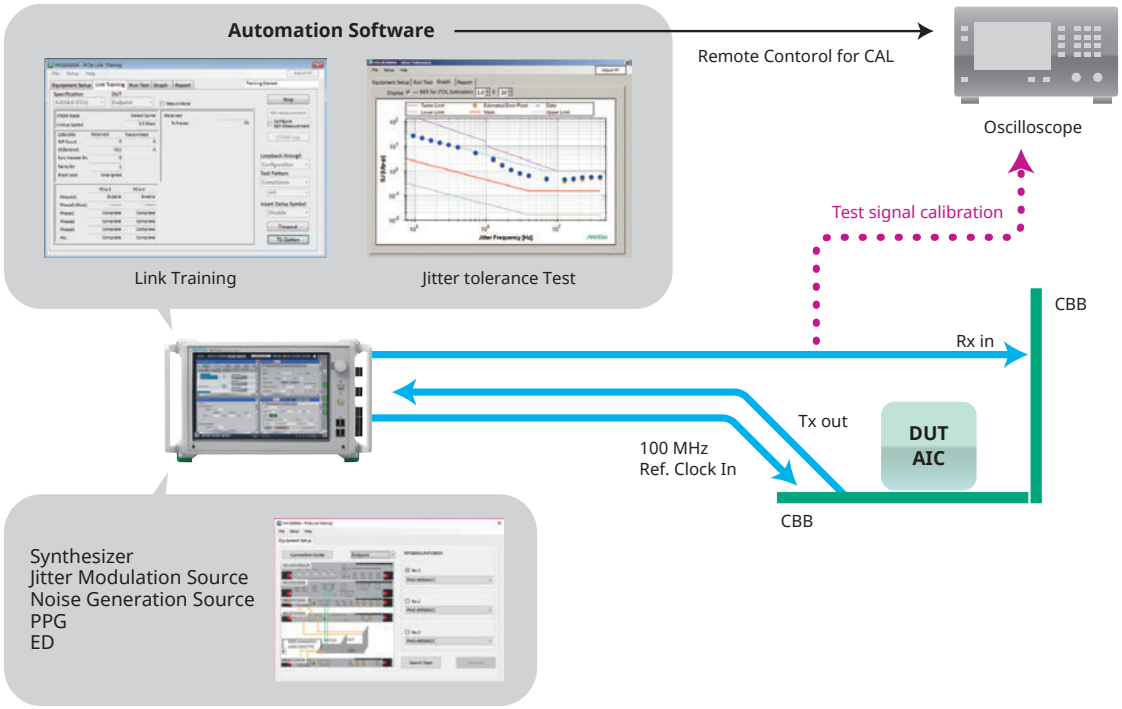
Automatic measurement of CTS-compliant Thunderbolt devices

Calibration Setting and Measurement Screens

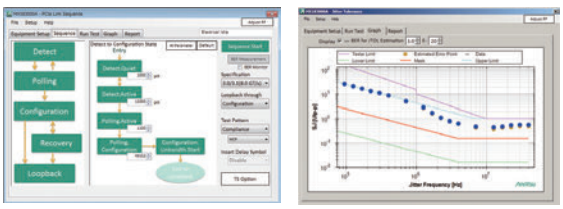
High-Speed Serial Data Test Solution MX183000A Application Examples

PCI Express Device Evaluation Setup MP1900A



Required Functions

- Loopback State Setting Function
- Jitter Tolerance Function
- Automatic Receiver Test Function
- Link Training Function
- Supports Common/Separate Clock Architecture



PCIe Link Sequence Generate Screen

Link Training Function

The PCI Express receiver test requires establishment of the Link status using LTSSM before performing the DUT BER test. Installing the PCIe Link Training MX183000A-PL021 option in the MP1900A supports verification of the Link status required for measurement. Additionally, the PCIe Link Training option has an LTSSM Analysis function for troubleshooting problems the Link status cannot be configured.

Receiver Jitter Tolerance Test

- SJ/RJ required for evaluating PCI Express 4.0 devices can be impressed to support PHY device Jitter tolerance tests.
- Device margins can be verified using low-rate BER estimates.
- Measurement results can be saved as HTML or CSV format reports.

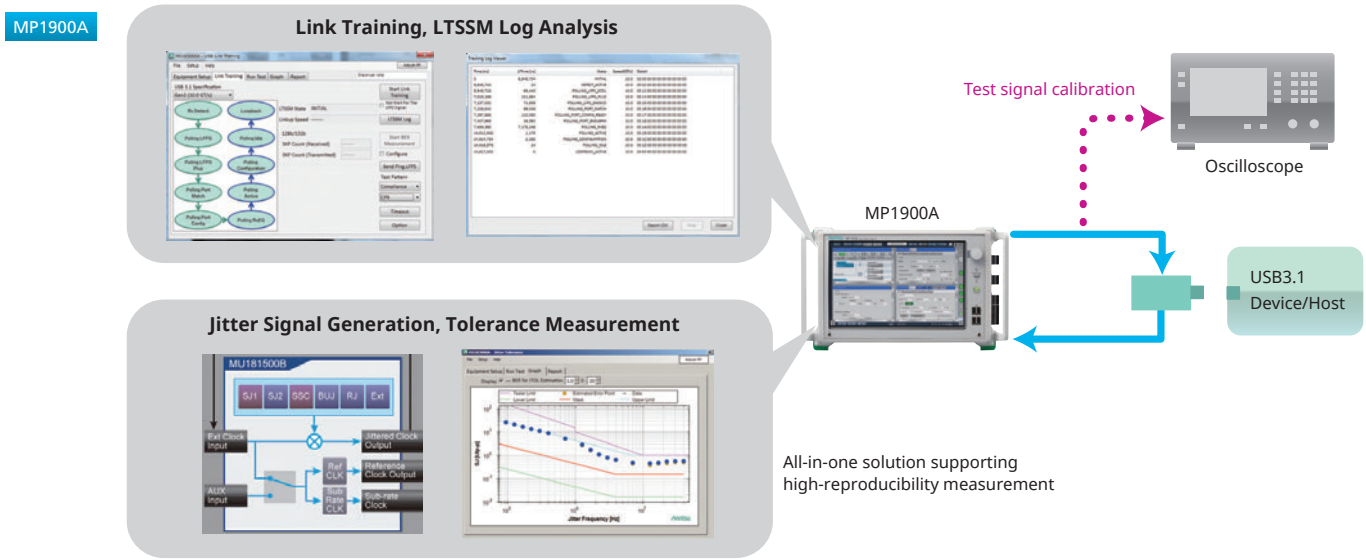
Event Trigger Generation Function

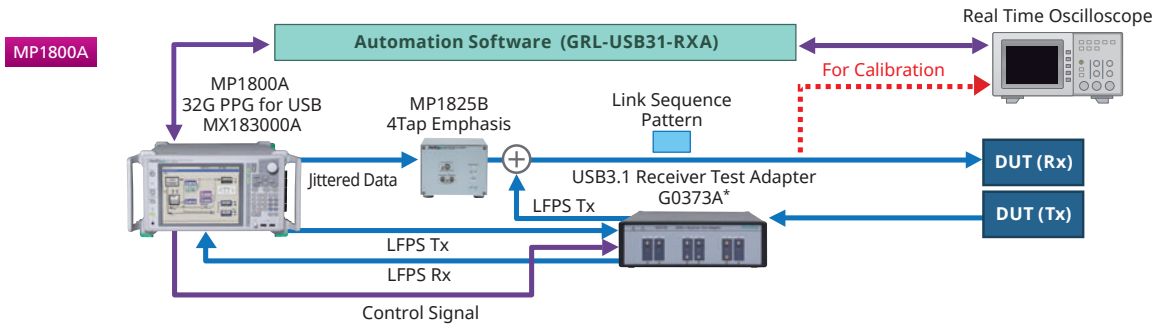
The PCI Express Gen3 and Gen4 standards require dynamic Link equalization in the Recovery state to be completed within 500 ns. The MP1900A supports Tx response time measurements by generating a trigger at a preset change request timing. In addition, generating a trigger at the LTSSM state transition timing enables precision monitoring of the transient signal at this time, supporting analysis of genuine factors when unable to establish the Link state.

*: Support only MP1800A
The GRL-PCIE4-BASE-RXA software is a Granite River Labs product.

High-Speed Serial Data Test Solution MX183000A Application Examples

USB Device Evaluation Setup





*: G0373A is used for LFPS (Low Frequency Periodic Signal) generation and BER measurement.

Required Functions

- Loopback State Setting Function
- Jitter Tolerance Function
- Automatic Receiver Test Function
- Link Training Function

Supported Standards: USB3.1 Gen1 and Gen2

DUT	Link Sequence Generation	Jitter Tolerance Test
Host Device	Supported	Supported

Link Training Function

The Link status required for measurement can be configured automatically using the MX183000A and options.

- The test mode can be transitioned to the Loopback mode required for evaluating USB3.1 Gen1 and Gen2 devices (MX183000A-PL012).

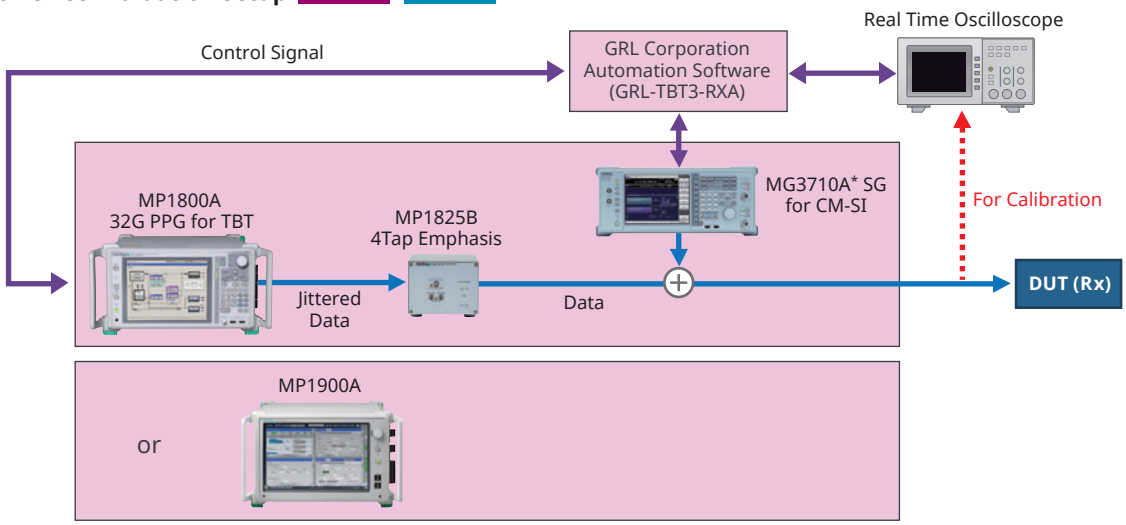
The Link Training option (MX183000A-PL022) has an LTSSM Analysis function for troubleshooting problems the Link status cannot be configured.

Receiver Jitter Tolerance Test

Jitter Tolerance tests can be automated using the MX183000A-PL001 software to help shorten the design validation time.

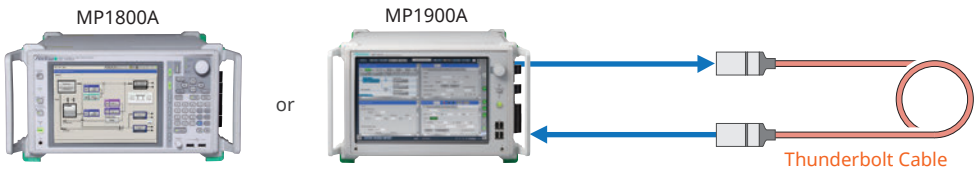
High-Speed Serial Data Test Solution MX183000A Application Examples

Thunderbolt Device Evaluation Setup MP1800A MP1900A



*: The MG3710A is used at common mode noise loads.

Thunderbolt Cable Evaluation Setup MP1800A MP1900A



Required Functions

- 20 Gbit/s PPG
- Stressed Signal Calibration Function
- Jitter Tolerance Function

Measurement Item	Supported Software
Stressed Signal Calibration	GRL-TBT3-RXA (Thunderbolt 3)
Jitter Tolerance Test	GRL-TBT3-RXA (Pass/Fail) Evaluation

Supported Standards: Thunderbolt 2/3

DUT	Jitter Tolerance Test
Host Device	Supported

Supports Thunderbolt 3

Supports Thunderbolt 3 specified bit rates (20G)

Stressed Signal Calibration

GRL Automation Software supports automatic stressed signal calibration as specified by Thunderbolt 3 (USB Type-C Thunderbolt Alternate Mode Electrical Host/Device Compliance Test Specification).

Stressed Signal Input Test

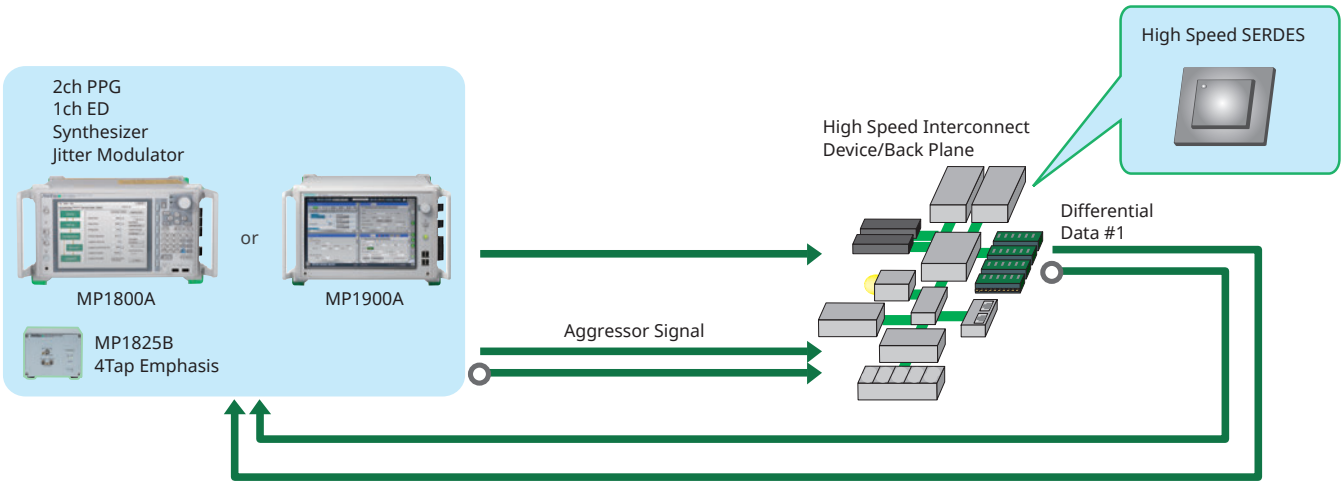
- Supports Rx BER measurements required by Host/Device compliance test
- Supports automatic Rx test using Tenlira scripts
- Supports automatic Pass/Fail measurement for Rx stressed signal tests

Receiver Test

Calibration and the Jitter Tolerance test can both be automated using the GRL-TBT3-RXA software. Automation helps cut design verification times.

High-Speed Serial Data Test Solution MX183000A Application Examples

30 Gbit/s Band Ultrafast Interconnect Evaluation MP1800A MP1900A



Required Test Items

- 32.1 Gbit/s Multi-channel signal generation
- Jitter Tolerance test
- Emphasis efficiency check
- Crosstalk test

Multi-channel

Along with support for multi-channels, the bit rate of devices such as back planes of high-performance servers is becoming increasingly faster. The MP1800A and MP1900A supports generating both the Victim signal with controlling Emphasis and the Aggressor signal for crosstalk testing simultaneously. The MP1800A and MP1900A offers multi-channel measurements for TRx devices such as Transceiver, SERDES and Clock Data Recovery (CDR).

Skew and Crosstalk Effect Check

Processing high speed digital signals requires both logic tests and actual equipment tests. The MP1800A and MP1900A supports both pattern synchronization and phase adjustment functions, permitting easy tests of Rx device skew tolerance and crosstalk effects.

Jitter Tolerance Test

Jitter Tolerance tests supporting various standards can be run by simultaneously impressing SJ (2 tone), RJ, BUJ, and SSC up to 32.1 Gbit/s using the MX183000A-PL001 and MU185000B Jitter modulation sources.
The Eye opening of signals passing through the back-plane is degraded by loss in the board traces.

Software

Item		PCI Express	USB	Thunderbolt	General
Calibration		MP1900A *1	GRL-USB31-RXA MP1800A MP1900A *1	GRL-TBT3-RXA MP1800A MP1900A *1	—
Link Sequence Generation		MX183000A-PL011 MP1900A	MX183000A-PL012 MP1800A	—	—
Link Training		MX183000A-PL021 MP1900A	MX183000A-PL022 MP1900A	—	—
Jitter Tolerance Test	Pass/Fail	—	GRL-USB31-RXA MP1800A	GRL-TBT3-RXA MP1800A	—
	Margin	MX183000A-PL001 MP1900A	MX183000A-PL001 MP1800A MP1900A	—	MX183000A-PL001 MP1800A MP1900A

*1: Please Contact our Sales Section about MP1900A support.

On Using VISA*2

For customers with MP1800A/MP1900A

The National Instruments™ (NI hereafter) NI-VISA*3 software must be installed to use the MX183000A (this product hereafter).
We recommend using NI-VISA saved on the product USB memory stick.
Customers may only use NI-VISA saved on the product memory stick. NI-VISA on the memory stick may not be used for other applications with other products.
When uninstalling this product from the controller PC, etc., also uninstall NI-VISA from the USB memory.

For customers with MT1810A

The National Instruments™ (NI hereafter) NI-VISA software must be installed to use the MX183000A (this product hereafter).
Customers must provide their own copy of NI-VISA.
Since the MT1810A has no built-in NI licensed hardware, NI-VISA is not bundled with the MT1810A.

*2: Abbreviation for Virtual Instrument Software Architecture. This is I/O software for remote control of measuring instruments via GPIB, Ethernet and USB interfaces.
*3: NI-VISA was developed by National Instruments for VXI Plug&Play Alliance standards compliant I/O interfaces.
National Instruments™, NI™, and NI-VISA™ are registered trademarks of National Instruments Corporation.

Configurations

Model	Name	PCI Express Gen3/4	USB3.1	Thunderbolt
MP1900A	Signal Quality Analyzer-R	1	1	1
MU181000B	12.5 GHz 4 Port Synthesizer	1	1	1
MU181000B-002	SSC Extension	1		1
MU181500B	Jitter Modulation Source	1	1	1
MU195020A	21G/32G bit/s SI PPG	1	1	1
MU195020A-010	1ch Data Output	1	1	1
MU195020A-011	1ch 10Tap Emphasis	1	1	1
MU195040A	21G/32G bit/s SI ED	1	1	
MU195040A-010	1ch ED	1	1	
MU195040A-011	1ch CTLE	1	1	
MU195040A-022	Clock Recovery	1	1	
MU195050A	Noise Generator	1	1*1	1
MX183000A-PL021	PCIe Link Training	1		
MX183000A-PL022	USB Link Training		1	

Model	Name	USB3.1	Thunderbolt
MP1800A	Signal Quality Analyzer	1	1
MP1800A-002	LAN	1	1
MP1800A-007	OS Upgrade to Windows 7	1	1
MP1800A-015	4-Slot for PPG and/or ED	1	1
MP1800A-032	32 Gbit/s PPG and/or ED Support	1	1
MU181000B	12.5 GHz 4port Synthesizer	1	1
MU181000B-001	Jitter Modulation		(1)
MU181500B	Jitter Modulation Source	1	1
MU183020A	28G/32G bit/s PPG	1	1
MU183020A-012	1ch 2 V Data Output	1	1
MU183020A-030	1ch Data Delay	1	1
MU183040B	28G/32G bit/s ED		
MU183040B-010	1ch ED		
MU183040B-022	2.4G to 28.1G bit/s Clock Recovery		
MP1825B	4Tap Emphasis	1	1
MP1825B-002	28 Gbit/s Operation	1	1
MG3710A*2	Vector Signal Generator		1
MG3710A-002	High Stability Reference Oscillator		1
MG3710A-029	OS Upgrade to Windows 7		1
MG3710A-036	1stRF 100 kHz to 6 GHz		1
MG3710A-041	High Power Extension for 1stRF		1
MG3710A-066	2ndRF 100 kHz to 6 GHz		1
MG3710A-071	High Power Extension for 2ndRF		1
MX183000A-PL011	PCIe Link Sequence		
MX183000A-PL012	USB Link Sequence	1	
CLE1000 Variable ISI Channel (ARTEK Corp.)*3			
G0373A*4	USB3.1 Receiver Test Adapter	1	

*1: Not required when using Pick Off Tee J1510A (2 pcs)
*2: For generating either common mode noise or differential mode noise
*3: For ISI load test
*4: For generating LFPS Signal/BER measurement

MP1800A

PCI Express Configuration (J1722A)

Model	Name	Qty.
J1398A	N-SMA ADAPTOR	4
K241C	Splitter	2
41KC-3	Fixed Attenuator 3 dB	2
41KC-6	Fixed Attenuator 6 dB	2
41KC-20	Fixed Attenuator 20 dB	2
J1510A	Pick OFF Tee	2
J1625A	Coaxial Cable, 1 m (SMA connector)	6
J1551A	Coaxial Skew Match Cable (0.8 m, K connector)	2
J1715A	Coaxial Skew Match Cable (0.1 m, SMP-J, SMA-J)	4
K261	DC Block	2

USB Configuration (J1721A)

Model	Name	Qty.
J1510A	Pick OFF Tee	2
J1625A	Coaxial Cable, 1 m (SMA connector)	3
J1551A	Coaxial Skew Match Cable (0.8 m, K connector)	2
J1624A	Coaxial Cable 0.3 m (SMA Connector)	2

Compliance Test Component Set (J1724A)

This component set supports PCI Express, USB and Thunderbolt Configuration.

Model	Name	Qty.
J1398A	N-SMA ADAPTOR	4
41KC-3	Fixed Attenuator 3 dB	2
41KC-6	Fixed Attenuator 6 dB	2
41KC-20	Fixed Attenuator 20 dB	2
K241C	Splitter	2
J1510A	Pick OFF Tee	2
J1551A	Coaxial Skew Match Cable (0.8 m, K connector)	2
J1625A	Coaxial Cable, 1 m (SMA connector)	6
J1715A	Coaxial Skew Match Cable (0.1 m, SMP-J, SMA-J)	4
K261	DC Block	2
J1624A	Coaxial Cable 0.3 m (SMA Connector)	2

Thunderbolt Configuration (J1723A)

Model	Name	Qty.
J1398A	N-SMA ADAPTOR	2
41KC-6	Fixed Attenuator 6 dB	2
1510A	Pick OFF Tee	2
J1625A	Coaxial Cable, 1 m (SMA connector)	2
J1551A	Coaxial Skew Match Cable (0.8 m, K connector)	2
J1715A	Coaxial Skew Match Cable (0.1 m, SMP-J, SMA-J)	2
K261	DC Block	2

Operation Conditions

Install Destination	MP1800A/MP1900A or PC
PC Specifications	OS: English or Japanese Windows 7 Professional/Enterprise/Ultimate CPU: 1 GHz min. Memory: 1 GB min. (for Windows 7, 32-bit) 2 GB min. (for Windows 7, 64-bit) Hard Disk: Free space 2 GB min. Remote Interface: Ethernet (10BASE-T, 100BASE-TX) Display: Resolution 800 × 600 min., 32-bit color
Control Target	MP1800A, MP1900A or MT1810A Required Options: MP1800A-02 LAN, MP1800A-07 OS Upgrade Windows 7 (MP1800A only), MP1800A-32 32 Gbit/s PPG/ED Support Controlled Units: 3 units max. Version: MX180000A Installer Version 8.02.00 or later

Sequence Tab (PCIe: MX183000A-PL011)

Sequence (Start/Stop/Unlink)	Sends sequence set at Editor; sends test pattern continuously after sending Link Sequence
BER Measurement	Starts BER measurement when clicking button after sending sequence
BER Monitor	OFF/ON
LTSSM State	Detect, Polling, Configuration, Recovery, Loopback
Specification	1.0/1.1(2.5 GT/s), 2.0(5 GT/s), 3.0/3.1(8 GT/s), 4.0(16 GT/s)
Loopback through	Configuration/Recovery
Test Pattern	Compliance/PRBS
Compliance	MCP/CP
PRBS	PRBS7, PRBS9, PRBS10, PRBS11, PRBS15, PRBS20, PRBS23, PRBS31
Inset Delay Symbol	Disable/Enable
Rev1.0/1.1 Configuration	(Detect.Quite, Detect.Active, Polling.Active, Polling.Configuration, Loopback.Entry) 1 to 1000000, 1 steps
Rev2.0 Configuration	(Detect.Quite, Detect.Active, Polling.Active, Polling.Configuration, Loopback.Entry (2.5G), Loopback.Entry (Electrical Idle), Loopback.Entry (5G)) 1 to 1000000, 1 steps
Rev2.0 Recovery	(Detect.Quite, Detect.Active, Polling.Active, Polling.Configuration, Configuration Linkwidth.Start, Configuration Linkwidth.Accept, Configuration Lane.Wait, Configuration Lane.Accept, Configuration Complete, Configuration Idle, Recovery RcvrLock, Recovery RcvrCfg (EQTS2), Recovery Speed, Recovery RcvrLock, Recovery RcvrCfg (TS2), Loopback.Entry (5G)) 1 to 1000000, 1 steps
Rev3.0/3.1 Configuration	(Detect.Quite, Detect.Active, Polling.Active, Polling.Configuration, Loopback.Entry (2.5G), Loopback.Entry (Electrical Idle), Loopback.Entry (8G)) 1 to 1000000, 1 steps
Rev3.0/3.1 Recovery	(Detect.Quite, Detect.Active, Polling.Active, Polling.Configuration, Configuration Linkwidth.Start, Configuration. Linkwidth.Accept, Configuration Lane.Wait, Configuration Lane.Accept, Configuration Complete, Configuration Idle, Recovery RcvrLock, Recovery RcvrCfg (EQTS2), Recovery Speed (8G), Recovery RcvrLock, Recovery Equalization Phase1, Recovery RcvrLock, Recovery RcvrCfg (TS2), Loopback.Entry (8G)) 1 to 1000000, 1 steps
Rev4.0 Recovery: MX183000A-PL011	(Detect.Quite, Detect.Active, Polling.Active, Polling.Configuration, Configuration Linkwidth.Start, Configuration. Linkwidth.Accept, Configuration Lane.Wait, Configuration Lane.Accept, Configuration Complete, Configuration Idle, Recovery RcvrLock, Recovery RcvrCfg (EQTS2), Recovery Speed(8G), Recovery RcvrLock, Recovery Equalization Phase1, Recovery RcvrLock, Recovery RcvrCfg (TS2), Recovery Idle, Recovery RcvrLock, Recovery RcvrCfg (EQTS2), Recovery Speed (16G), Recovery RcvrLock, Recovery Equalization Phase1, Recovery RcvrLock, Recovery RcvrCfg (TS2), Loopback.Entry (16G)) 1 to 1000000, 1 steps

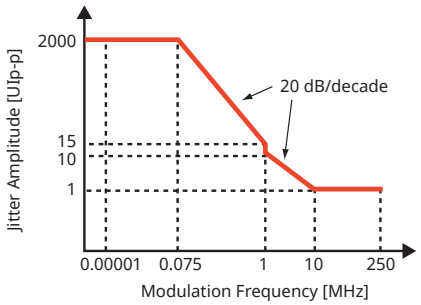
TS Option	TS Parameter FTS, Link Number, Lane Number: 0 to 255, 1 steps Full Swing, Low Frequency: 12 to 63, 1 steps SRIS: Disable Disable Scrambling: OFF/ON Reset EIEOS Interval: Disable/Enable
SKP	SKP Insert: Enable/Disable SKP Length (128b/130b): 8 to 24 Symbol, 4 steps SKP Length (8b/10b): COM + 1 to 5, 1 steps SKP Interval (128b/130b): 187 to 750, 1 steps SKP Interval (8b/10b): 768 to 3076, 2 steps
Send TS	Polling.Active: TS1/EQTS1 Loopback.Ectry: TS1/EQTS1
Rev3.x/Rev4.0 Preset	Downstream Preset(DE, PS [dB]): P7 : –6.0, 3.5 Preset Hint: –6 dB Precursor, Cursor, Postcursor: 0 Upstream Usepreset: Preset Preset(DE, PS [dB]): P7 : –6.0, 3.5 Preset Hint: –6 dB Precursor, Cursor, Postcursor: 0

Sequence Tab (USB: MX183000A-PL012)

LTSSM State	eSS.Inactive, Rx.Detect, Polling, Loopback
USB3.1 Specification	Gen1 (5.0 Gbit/s), Gen2 (10.0 Gbit/s)
Test Pattern	Compliance/USER
CPx	Gen1: CP0 D0.0, CP1 D10.2, CP2 D24.3, CP3 K28.5, CP4 LFPS, CP5 K28.7*, CP6 K28.7* Gen2: CP9
Gen1	Rx.Detect.Active (Idle), Polling.RxEQ, Polling.Active (TS1), Polling.Configuration (TS2), Polling.Idle 1 to 1000000, 1 steps Polling.LFPS 100 to 1000000, 10 steps
Gen2	Rx.Detect.Active (Idle), Polling.RxEQ, Polling.Active (TS1), Polling.Configuration (TS2), Polling.Idle 1 to 1000000, 1 steps Polling.LFPS (SCD1) 162 to 1000000, 1 steps Polling.LFPSPlus(SCD2) 172 to 1000000, 1 steps Polling.PortMatch (PHY Capability LBPM), Polling.PortConfig (PHY Ready LBPM) 2 to 1000000, 1 steps
Option	Loopback: Asserted Disable Scrambling: OFF/ON
SKP	SKP Insert: Enable/Disable Symbol Length (128b/132b): 8 to 40, 2 steps Symbol Length (8b/10b): 2 to 6, 2 steps SKP Interval (128b/132b): 20 to 80, 1 steps SKP Interval (8b/10b): 176 to 708, 2 steps tPeriod: 20 ns Duty: 50%
WarmReset	tBurst: 100 ms
LFPS	tBurst: 1.000 µs
SuperSpeed	tRepeat: 10.000 µs
SuperSpeedPlus	Logic0: 7.000 µs Logic1: 12.000 µs SCD1: 33.000 µs SCD2: 43.000 µs
LBPM	tLFPS-1: 1.500 µs tLFPS-0: 0.700 µs tPWM: 2.200 µs

*: The actual output de-emphasis setting is not changed even when selecting CP5 and CP6.

Run Test Tab (MX183000A-PL001)

Run Test/Stop Test	Starts and stop Jitter Tolerance Test
Jitter Tolerance Table	JTOL Measurement Point Setting Sets measured SJ modulation frequency and Pass/Fail modulation degree (UI), and set search modulation range Jitter Frequency Setting Range Sets each of Jitter Freq. [Hz], Mask [UI], Upper Limit [UI], Lower Limit [UI], Upper Ratio, Lower Ratio Setting range depends on Jitter modulation source MU181500B Jitter Amplitude Setting Range  As in above table. However, the Jitter frequency and amplitude that can be measured change according to the controller and MU181500B clock frequency setting. Set All Limit The Jitter Tolerance Table Upper Limit and Lower Limit values are reset at the ratio corresponding to the value set at Mask. The reset ratio is set at Upper Ratio and Lower Ratio. Upper Ratio: 1.000 to 1000, 0.001 steps Lower Ratio: 0.001 to 1.000, 0.001 steps Measurement Sequence: From higher Freq. side, From lower Freq. side
JTOL Setting	Detection Unit: Error Rate, Error Count, Estimate Error Threshold: 1E–3 to 1E-12, E–1 steps Error Count: 0 to 10000000, 1 steps BER for JTOL Estimation: 1.0E–20 to 9.9E–9
Auto Search	OFF/FINE/COARSE
Search	Direction Search: Binary, Downwards Linear, Downwards Log, Upwards Linear, Upwards Log, Binary + Linear Step: At Downwards/Upwards Linear selection Jitter Freq. ≤ 100 kHz 0.001 to 2000.000 0.001 steps 100k < Jitter Freq.≤ 1 MHz 0.001 to 200.000 0.001 steps 1M < Jitter Freq.≤ 10 MHz 0.001 to 15.000 0.001 steps 10 MHz < Jitter Freq. 0.001 to 1.000 0.001 steps Ratio: At Downwards/Upwards Log selection Jitter Freq.≤ 100 kHz, 100k < Jitter Freq.≤ 1 MHz, 1M < Jitter Freq.≤ 10 MHz, 10 MHz < Jitter Freq. 0.01 to 1.00 0.01 steps
Timer [sec.]	Waiting, Setting: 1 to 99 s, 1 s steps Gating: 1 to 86400 s, 1 s steps

Graph Tab (MX183000A-PL001)

Display	OFF/ON
BER for JTOL Estimation	1.0E–20 to 9.9E–9, 0.1 steps, E–1 steps

Report Tab (MX183000A-PL001)

Make HTML/Make CSV	Displays Jitter Tolerance results as HTML or CSV

MX183000A-PL021

Link Training Tab	Supports PCI Express Link Training (Gen1 to Gen4)

MX183000A-PL022

Link Training Tab	Supports USB Link Training (USB 3.1 Gen1 and Gen2)

High-Speed Serial Data Test Solution MX183000A Related Instruments

Signal Quality Analyzer-R MP1900A

2.4 Gbit/s to 32.1 Gbit/s

Support 400 GbE and PCIe Gen4/5

- 512 Gbit/s max. transmission capacity, one main frame expandable to 16 ch (filling 8 slots with 32 Gbit/s 2 ch PPG)
- All-in-one support for both high-speed Ethernet and PCI Express interface tests
- Wideband 32 Gbit/s SI PPG/ED
  - Bit rate of 2.4 Gbit/s to 32.1 Gbit/s
  - NRZ/PAM4 Support
  - 10Tap Emphasis and Variable ISI Function
  - Multi-band CTLE (28 Gbit/s, 16 Gbit/s, 8 Gbit/s bandwidths)
  - Low Intrinsic Jitter output of random Jitter 115 fs rms (typ.)
  - High-sensitivity Data input of 15 mV (Eye Height) (typ.)
  - 1 ch/2 ch Selection
- PCI Express/USB Link Training and LTSSM analysis
- Jitter Addition, Jitter Tolerance measurement functions (SJ/RJ/BUJ/SSC)
- Voltage Noise Addition function (Common/Differential/White Noise)

The MP1900A is a high-performance BERT with excellent expandability for supporting Physical layer evaluations of these high-speed interfaces. The all-in-one design is ideal for early stage R&D evaluations of all interfaces covering next-generation Ethernet networks to bus interconnects.

Signal Quality Analyzer MP1800A Series

0.1 Gbit/s to 32 Gbit/s

Compact, High-Performance BER Tester for Measurements from 0.1 Gbit/s to 32 Gbit/s

- Evaluates 100 GbE optical modules, 32G FC, InfiniBand EDR, 100G, DP-QPSK, and PAM signals
- Uses PPG synchronization function to support Jitter, crosstalk, skew, and emphasis tests required by faster, multi-channel interconnects market
- Uses 3.5 Vp-p high-amplitude waveforms and variable crossover point function for EML direct-drive evaluations

The MP1800A is ideal for PHY-layer evaluations of optical modules and high-speed devices from 0.1 Gbit/s to 32.1 Gbit/s. Additionally, when used in combination with a 56G/64 Gbit/s MUX/DEMUX, it supports BER tests up to 64.2 Gbit/s. The plug-in module design accommodates a selection of various modules and options for a customized configuration meeting every application requirement.

4Tap Emphasis MP1825B

1 Gbit/s to 14.1 Gbit/s, 1 Gbit/s to 32.1 Gbit/s

Evaluates Serial Interface Characteristics using Pre-Emphasis Signal

- Supports Pre-emphasis for up to 4 taps
- Provides two operating frequencies (14.1 Gbit/s and 32.1 Gbit/s)
- Supports Jitter transparency
- Supports small remote-head operation

The MP1825B is a compact 4Tap Pre-Emphasis supporting bit rates up to 32.1 Gbit/s; it is ideal for evaluating the characteristics of many high-speed interfaces, such as PCI Express, USB, backplane Ethernet, InfiniBand EDR, CEI-28G-VSR, 32G FC, etc., requiring pre-emphasis signals, because it can easily change the pre-emphasis waveform amplitude, offset, and amplitude for each tap. It plays a key role in accurate evaluation of high-speed interconnects by compensating for attenuation of the signal level as it passes through the PCB, or by compensating for a degraded Eye opening with high-speed Tr/Tf.

High-Speed Serial Data Test Solution MX183000A Ordering Information

Please specify the model/order number, name and quantity when ordering.
The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

Model/Order No.	Name
	Main Frame
MP1800A	Signal Quality Analyzer
MP1900A	Signal Quality Analyzer-R
MP1825B*1	4Tap Emphasis
MG3710A	Vector Signal Generator
	Options
MP1800A-001	GPIB
MP1800A-002	LAN
MP1800A-007	OS Upgrade to Windows 7
MP1800A-015	4-Slot for PPG and/or ED
MP1800A-032	32 Gbit/s PPG and/or ED Support
MP1825B-002*1	28 Gbit/s Operation
MG3710A-002	High Stability Reference Oscillator
MG3710A-029	OS Upgrade to Windows 7
MG3710A-036	1stRF 100 kHz to 6 GHz
MG3710A-041	High Power Extension for 1stRF
MG3710A-066	2ndRF 100 kHz to 6 GHz
MG3710A-071	High Power Extension for 2ndRF
	Module
MU181000B	12.5 GHz 4port Synthesizer
MU181500B	Jitter Modulation Source
MU183020A	28G/32G bit/s PPG
MU183040B	28G/32G bit/s High Sensitivity ED
MU195020A	21G/32G bit/s SI PPG
MU195040A	21G/32G bit/s SI ED
MU195050A	Noise Generator
	Module Options
MU181000B-001	Jitter Modulation
MU181000B-002	SSC Extension
MU183020A-012	1ch 2 V Data Output
MU183020A-013	1ch 3.5V Data Output
MU183020A-023	2ch 3.5V Data Output
MU183020A-030	1ch Data Delay
MU183021A-013	4ch 3.5V Data Output
MU183040B-010	1ch ED
MU183040B-022	2.4G to 28.1G bit/s Clock Recovery
MU195020A-010	1ch Data Output
MU195020A-011	1ch 10Tap Emphasis
MU195020A-040	1ch Variable ISI
MU195020A-041	2ch Variable ISI
MU195040A-010	1ch ED
MU195040A-011	1ch CTLE
MU195040A-022	Clock Recovery
	Software
MX183000A*2	High-Speed Serial Data Test Software
	Software Options
MX183000A-PL001	Jitter Tolerance Test
MX183000A-PL011	PCIe Link Sequence
MX183000A-PL012	USB Link Sequence
MX183000A-PL021	PCIe Link Training
MX183000A-PL022	USB Link Training

Model/Order No.	Name
	Optional Accessories
W3813AE	MX183000A Operation Manual
41KC-3	Fixed Attenuator 3 dB
41KC-6	Fixed Attenuator 6 dB
41KC-20	Fixed Attenuator 20 dB
J1343A	Coaxial Cable 1.0 m (SMA, DC to 18 GHz)
J1349A	Coaxial Cable 0.3 m (SMA, DC to 18 GHz)
J1359A	Coaxial Adapter (K-P, K-J, SMA)
J1398A	N-SMA ADAPTOR
J1508A	BNC-SMA Connector Cable (30 cm)
J1510A	Pick OFF Tee
J1551A	Coaxial Skew Match Cable (0.8 m, K connector)
J1615A	Coaxial Cable Set (Jitter-PPG-Emphasis)
J1627A	GND Connection Cable
J1624A	Coaxial Cable 0.3 m (SMA Connector)
J1625A	Coaxial Cable 1 m (SMA Connector)
J1632A	Terminator (SMA)
J1715A	Coaxial Skew Match Cable (0.1M, SMP-J, SMA-J)
K220B	Coaxial Adapter
K241C	Power Splitter
K261	DC Block
K250	Bias T
Z1927A	USB Measurement Kit
J1721A	USB Measurement Component Set
J1722A	PCIe Measurement Component Set
J1723A	TBT Measurement Component Set
J1724A	Compliance Test Component Set
G0373A*3	USB3.1 Receiver Test Adapter
G0374A*3	64Gbaud PAM4 DAC

∗1: MP1825B is not RoHS compliant.
∗2: MX183000A include PAM control software (Free).
∗3: The warranty period shall be 1 year under normal use.
Repair by exchange for new during the warranty period shall be limited to one instance.
Repair using new spare parts shall be charged after the warranty period has expired.

Moreover, Anritsu Corporation will deem this warranty void when:

- When new spare parts can no longer be easily obtained when more than 5 years have elapsed after manufacture.